

1 CLAIMS:

2 1. In a capacitor-over-bit line memory array, a method of
3 forming a conductive capacitor plug comprising extending conductive
4 material from proximate a substrate node location to a location
5 elevationally above all conductive material of an adjacent bit line.

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7 2. The method of claim 1, wherein the extending comprises
8 etching a contact opening through insulative material after forming said
9 bit line and forming conductive material within the contact opening.

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11 3. The method of claim 2, wherein the forming of the
12 conductive material comprises forming a storage capacitor at least
13 partially within the contact opening.

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15 4. The method of claim 1, wherein the extending comprises
16 etching a contact opening through two separately-formed insulative
17 material layers, at least a portion of the contact opening being generally
18 self-aligned to said bit line, and forming conductive material within the
19 contact opening.

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21 5. The method of claim 1, wherein the array comprises a word
22 line elevationally below the bit line, and the extending comprises etching
23 a contact opening through insulative material and generally self-aligned
24 to both said bit line and said word line.

1 6. The method of claim 5, wherein the insulative material
2 comprises two or more separately-formed insulative material layers.

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4 7. The method of claim 1, wherein the extending comprises:
5 forming a patterned masking layer over the substrate and defining
6 an opening pattern over said substrate node location;
7 etching insulative material through the opening pattern sufficient
8 to form a contact opening after forming said bit line; and
9 forming conductive material within the contact opening.

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11 8. The method of claim 7, wherein said opening pattern is
12 formed over a plurality of substrate node locations over which individual
13 capacitors are to be formed.

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15 9. The method of claim 1, wherein said substrate node location
16 comprises a diffusion region, and the extending comprises:

17 etching a contact opening through insulative material to
18 substantially expose a portion of the diffusion region after forming said
19 bit line; and

20 forming conductive material within the contact opening and in
21 electrical communication with the diffusion region.

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23 10. The method of claim 9, wherein said insulative material
24 comprises two separately-formed layers of insulative material.

1 11. In a capacitor-over-bit line memory array, a method of
2 forming a capacitor contact opening comprising etching an opening
3 through a first insulative material received over a bit line and a word
4 line substantially selective relative to second insulative material covering
5 the bit line and the word line to a substrate location proximate the
6 word line in a self-aligning manner relative to both the bit line and the
7 word line.

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9 12. The method of claim 11, wherein the first insulative material
10 comprises separately-formed layers of insulative material.

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12 13. The method of claim 11, wherein the first insulative material
13 comprises two separately-formed layers of insulative material.

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15 14. The method of claim 11, wherein the second insulative
16 material separately encapsulates the bit line and the word line.

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18 15. The method of claim 11, wherein the substrate location
19 comprises a diffusion region, and the etching comprises outwardly
20 exposing the diffusion region.

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22 16. The method of claim 11, wherein the etching comprises
23 removing all of the first insulative material from over the bit line.
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1 17. The method of claim 11, wherein the etching comprises
2 forming a patterned masking layer over the first insulative material
3 defining an opening pattern, and etching the opening through the
4 opening pattern.

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6 18. The method of claim 11 further comprising forming
7 conductive material within the opening, the conductive material extending
8 to an elevation laterally proximate conductive portions of the bit line.

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10 19. The method of claim 11 further comprising forming
11 conductive material within the opening, the conductive material extending
12 to a location elevationally higher than any conductive portion of the bit
13 line.

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15 20. In a capacitor-over-bit line memory array, etching an array
16 of capacitor contact openings to elevationally below the bit lines after
17 forming the bit lines.

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19 21. The method of claim 20, wherein the etching comprises
20 etching openings down to proximate individual substrate diffusion regions.

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22 22. The method of claim 20, wherein the etching comprises
23 etching openings down to proximate individual word lines of the array.
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1 23. The method of claim 22, wherein the etching comprises
2 exposing individual substrate diffusion regions intermediate the word
3 lines.

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5 24. The method of claim 20, wherein etching comprises
6 selectively etching through first insulative material relative to second
7 insulative material covering portions of the bit lines.

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9 25. The method of claim 20, wherein the etching comprises
10 selectively etching through first insulative material relative to second
11 insulative material covering portions of the bit lines and word lines of
12 the array.

13
14 26. The method of claim 25, wherein the first insulative material
15 comprises a plurality of separately formed layers of first insulative
16 material.

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18 27. The method of claim 20 further comprising forming
19 conductive material within the contact openings, the conductive material
20 extending to at least laterally proximate conductive portions of the bit
21 lines.

1 28. The method of claim 20 further comprising forming
2 conductive material within the contact openings, the conductive material
3 extending elevationally higher than any conductive portions of the bit
4 lines.

5
6 29. A method of forming a capacitor-over-bit line memory array
7 comprising:

8 forming a plurality of word lines over a substrate, the word lines
9 having insulating material thereover;

10 forming a plurality of bit lines over the word lines, the bit lines
11 having insulating material thereover;

12 forming insulative material over the word lines and the bit lines,
13 the insulative material being etchably different from the insulating
14 material over the word lines and the insulating material over the bit
15 lines; and

16 selectively etching capacitor contact openings through the insulative
17 material relative to the insulating material over the bit lines and the
18 insulating material over the word lines, the openings being self-aligned
19 to both bit lines and word lines and extending to proximate the
20 substrate.

21
22 30. The method of claim 29, wherein the forming of the
23 insulative material comprises forming a plurality of layers of insulative
24 over at least one of the word lines and bit lines.

1 31. The method of claim 29, wherein forming of the insulative
2 material comprises forming one layer of insulative material over the
3 word lines, and after the forming of the bit lines, forming another layer
4 of insulative material over the bit lines.

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6 32. The method of claim 31 further comprising forming a
7 patterned masking layer over the insulative material defining a mask
8 opening, the mask opening being received over a plurality of substrate
9 locations over which the capacitor contact openings are to be etched,
10 and the etching of the capacitor contact openings comprises etching said
11 contact openings through said mask opening.

12
13 33. The method of claim 29 further comprising forming
14 conductive material within the contact openings, the conductive material
15 being formed to extend from proximate individual substrate diffusion
16 regions to at least locations which are elevationally coincident with
17 conductive material of the individual bit lines.

18
19 34. The method of claim 29 further comprising forming
20 conductive material within the contact openings, the conductive material
21 being formed to extend from proximate individual substrate diffusion
22 regions to locations elevationally higher than any conductive material of
23 any of the bit lines.

1 35. A method of forming a capacitor-over-bit line memory array
2 comprising:

3 forming a plurality of word lines over a substrate;

4 forming a plurality of bit lines over the word lines;

5 forming insulative material over the word lines and the bit lines;

6 and

7 after forming the bit lines, etching an opening through the
8 insulative material and outwardly exposing a diffusion region received
9 within the substrate proximate a word line.

10
11 36. The method of claim 35, wherein the forming of the
12 insulative material comprises forming two separate layers of insulative
13 material over the substrate, and the etching of the opening comprises
14 etching the two layers selectively relative to insulative coverings formed
15 over portions of both the bit lines and the word lines.

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17 37. The method of claim 35 further comprising forming
18 conductive material within the opening, the conductive material extending
19 from proximate the diffusion region to a location elevationally higher
20 than any conductive material of the bit lines.

1 38. A method of forming a memory array comprising in
2 sequence:

3 forming a plurality of conductive lines over a substrate;

4 forming a conductive bit line plug intermediate a pair of the
5 conductive lines;

6 forming a bit line in electrical communication with the conductive
7 bit line plug;

8 forming a conductive capacitor plug proximate one of the pair of
9 conductive lines, which capacitor plug extends away from the substrate
10 and terminates above conductive portions of the bit line; and

11 forming a capacitor over and in electrical communication with the
12 capacitor plug.

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14 39. The method of claim 38, wherein the memory array is a
15 capacitor-over-bit line memory array.

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17 40. The method of claim 38, wherein the bit line plug and bit
18 line comprise at least one common material.

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20 41. The method of claim 38, wherein the bit line plug and bit
21 line comprise at least one common material, said common material
22 being deposited in a common processing step.

1 42. The method of claim 38, wherein the forming of the
2 capacitor plug comprises forming said surface elevationally higher than
3 any conductive portion of the bit line.
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5 43. The method of claim 38 further comprising prior to the
6 forming of the conductive bit line plug, forming first insulative material
7 over the conductive lines, and wherein the forming of the conductive
8 capacitor plug comprises substantially selectively etching an opening into
9 the first insulative material relative to second insulative material over
10 the conductive lines.
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12 44. The method of claim 38 further comprising prior to the
13 forming of the conductive capacitor plug, forming first insulative material
14 over the bit line, and wherein the forming of the conductive capacitor
15 plug comprises substantially selectively etching an opening into the first
16 insulative material relative to second insulative material over the bit
17 line.
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1 45. The method of claim 38 further comprising:
2 prior to the forming of the conductive bit line plug, forming a
3 first layer of first insulative material over the conductive lines; and
4 prior to the forming of the conductive capacitor plug, forming a
5 second layer of first insulative material over the bit line,
6 wherein the forming of the conductive capacitor plug comprises
7 substantially selectively etching an opening into the first insulative
8 material relative to second insulative material over the conductive lines
9 and bit line.

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11 46. The method of claim 45, wherein the etching comprises
12 exposing a substrate diffusion region proximate the conductive lines.
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1 47. A method of forming a memory array comprising:
2 forming a plurality of word lines over a substrate, the word lines
3 being encapsulated with a first insulative material;
4 forming a second layer of a second insulative material over the
5 word lines, the second insulative material having a generally planar
6 uppermost surface;
7 patterning the layer of second insulative material to define a bit
8 line plug opening exposing a first substrate diffusion region between two
9 of the word lines;
10 forming conductive material over at least a portion of said second
11 insulative material and in electrical communication with the first
12 substrate diffusion region;
13 removing some of the conductive material over the substrate
14 diffusion region to form a bit line plug in said opening;
15 forming a bit line over the second insulative material and in
16 electrical communication with the bit line plug, the bit line being
17 encapsulated with a third insulative material;
18 forming a layer of a fourth insulative material over the bit line;
19 patterning the layer of fourth insulative material to define an
20 opening over a second substrate diffusion region, said second substrate
21 diffusion region being on an opposite side of one of two word lines
22 between which the bit line plug was formed to form an opening which
23 is generally self-aligned to both the word lines and the bit line; and
24

1 forming conductive material within said self-aligned opening and
2 extending to a location higher than the bit line.

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4 48. A method of forming a memory array comprising:

5 forming a plurality of word lines over a substrate, the word lines
6 having insulating material thereover;

7 forming a plurality of bit lines over the word lines, the bit lines
8 having insulating material thereover;

9 forming insulative material over the word lines and the bit lines,
10 the insulative material being etchably different from the insulating
11 material over the word lines and the insulating material over the bit
12 lines; and

13 selectively etching contact openings through the insulative material
14 relative to the insulating material over the bit lines and the insulating
15 material over the word lines, the openings being self-aligned to both bit
16 lines and word lines and extending to proximate the substrate.